SEMICONDUCTOR MEMORY DEVICE TESTABLE WITH A SINGLE DATA RATE AND/OR DUAL DATA RATE PATTERN IN A MERGED DATA INPUT/OUTPUT PIN TEST MODE

Abstract of the Disclosure

Provided is a semiconductor memory device testable with a single data rate (SDR) or a dual data rate (DDR) pattern in a merged data input/output pin (DQ) test mode. The device includes a first path circuit, a second path circuit, and a merged output generator configured to generate a merged data bit having a SDR and/or DDR pattern.